

MSPM0 I2C module introduction

— MSPM0 peripheral training series

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MCU level overview

—MSPM0Lxx series

MSPM0L13x3/4/5/6

1.62 - 3.6V
-40 to 125 C

CPU ARM Cortex-M0+ 32 MHz NVIC / 3-ch DMA	Power & Clocking POR / BOR / SVS Internal LF 32kHz (5%) Internal HF 4-32MHz (1%)	Precision Analog 12-bit SAR ADC 1Msps (1) ULP/HS Comparator (1) 8-bit reference DAC (1) Zero-drift chopper op-amps (2) General purpose amp (1) Internal ADC reference (2.5%) Temperature sensor
On-chip Memory 8, 16, 32 or 64 kB flash 2 or 4 kB SRAM	Communication UART w/ LIN (1) UART (1) SPI (1)	Timers General purpose 16-bit 2 CC (4) Windowed watchdog
Data Integrity & Security CRC accelerator (16 and 32 bit)	IO Up to 28 GPIO Up to 2 low Ib OPA inputs	
Programming & Debug ARM SWD interface ROM UART & I2C BSL	I2C (2) w/ FastMode+	

Ledged packages: SOT-16, VSSOP-20/28
 No-lead packages: WQFN-16, VQFN-24/32

32 MHz MCU with up to 64kB flash, 32 pins, 12-bit ADC, dual zero-drift OPA/PGA, COMP

—MSPM0Gxx series

MSPM0G350x/310x/150x/110x

1.62 - 3.6V
-40 to 125 C

CPU Arm Cortex-M0+ 80 MHz NVIC / MPU / 7-ch DMA	Power & Clocking POR / BOR / SVS External LF 32kHz XTAL External HF 4-48MHz XTAL Internal LF 32kHz (3%) Internal HF 4-32MHz (1%) PLL (up to 80 MHz)	Precision Analog 12-bit ADC 4Msps (9-ch) 12-bit ADC 4Msps (8-ch) Comparators w/ 8-bit DACs (3) 12-bit 1Msps buffered DAC (1) Zero-drift chopper op-amps (2) Internal reference (1.5%) General purpose amp (1) Temperature sensor
Accelerators Math (DIV, SQRT, TRIG, MAC)	On-chip Memory 32, 64, or 128 kB flash [ECC] 16 or 32 kB SRAM [ECC]	Timers Advanced control 16-bit 4 CC (1) Advanced control 16-bit 2 CC (1) General purpose 32-bit 2 CC (1) General purpose 16-bit 2 CC (2) Low power 16-bit 2 CC (2) Windowed watchdog (2) Real-time clock (1)
Data Integrity & Security CRC accelerator (16 and 32 bit) AES256 accelerator + TRNG	Communication UART w/ LIN (1) UART (3) SPI (2) CAN-FD (1)	
Programming & Debug ARM SWD interface UART & I2C bootloader	IO Up to 60 GPIO	
	I2C (2) w/ FastMode+	

Ledged packages: VSSOP-20/28, LQFP-48/64
 No-lead packages: VQFN-24/32/48, nFBGA-64, WCSP-28

80 MHz MCU with up to 128kB flash, 64 pins, advanced analog, AES/TRNG, CAN-FD

MSPM0 I2C module introduction

Key features

- Fast-mode Plus (Fm+) with a bit rate up to **1 Mbps**
- Independent 8-byte FIFOs for reception and transmission
- Dual target address capability
- Controller operation with arbitration, clock synchronization, multiple controller support
- Hardware support for SMBus and PMBus
- Hardware support for DMA with separate channels for transmitting and receiving

Application note

The following minimum functional clock frequencies are required when running certain I2C clock speeds:

Running mode	SCL Speed	I2C_CLK requirement
Standard mode	$\leq 100\text{kHz}$	$\geq 2\text{MHz}$
Fast mode	$\leq 400\text{kHz}$	$\geq 8\text{MHz}$
Fast mode plus	$\leq 1\text{MHz}$	$\geq 20\text{MHz}$

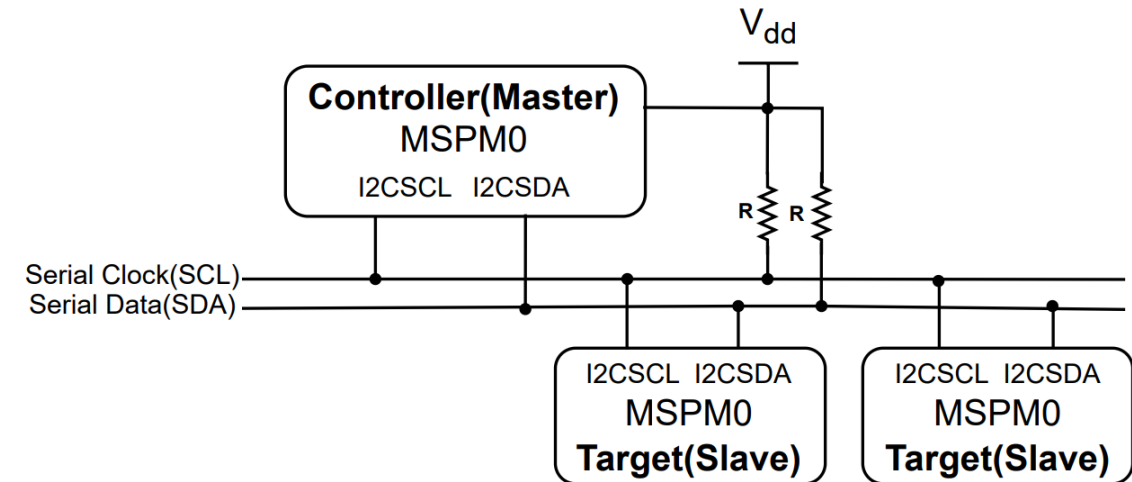


Fig1: I2C Typical Application

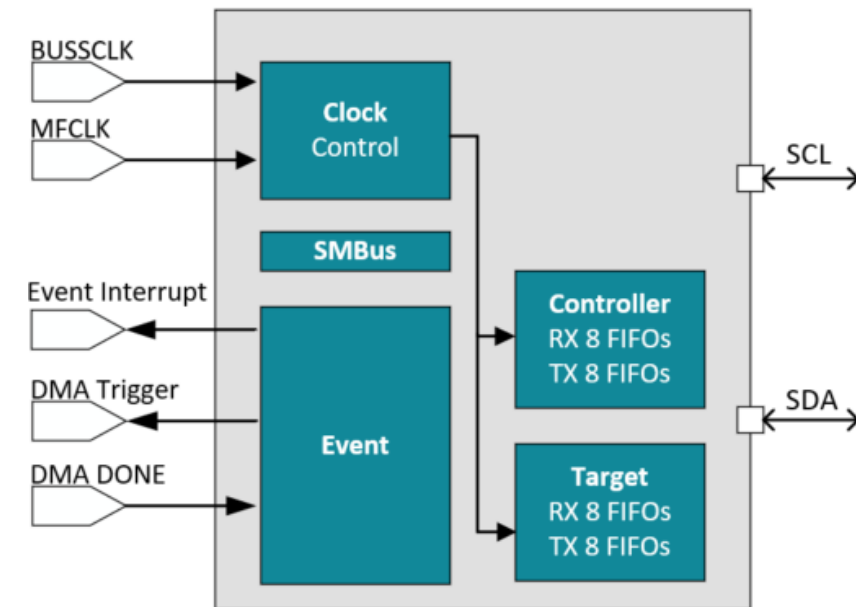


Fig2: MSPM0 I2C Block Diagram

I2C module quick start

Academy

[I2C introduction lab](#)

Driverlib Examples

[i2c_controller_rw_multibyte_fifo_interrupts](#)

[i2c_controller_rw_multibyte_fifo_poll](#)

[i2c_controller_target_dynamic_switching](#)

[i2c_multicontroller_arbitration](#)

[i2c_target_rw_multibyte_fifo_interrupts](#)

[i2c_target_rw_multibyte_fifo_interrupts_stop](#)

[i2c_target_rw_multibyte_fifo_poll](#)

Related links

[MSPM0 online resource](#)

[MSPM0 quick start guide](#)

[MSPM0 Sysconfig user's guide](#)

[MSPM0G350x datasheet](#)

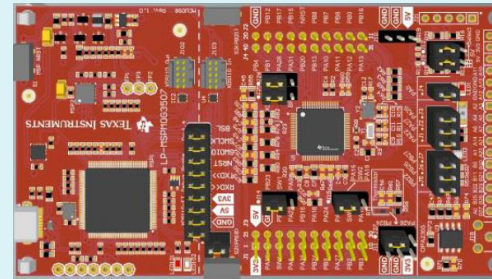
[MSPM0L13xx datasheet](#)

[MSPM0Gxx technical reference manual](#)

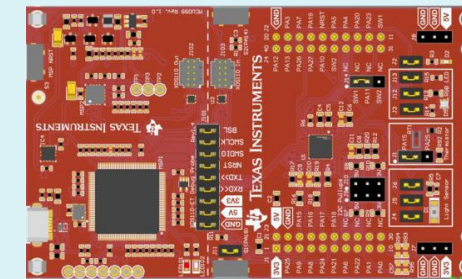
[MSPM0Lxx technical reference manual](#)

Launchpad

[LP-MSPM0G3507](#)



[LP-MSPM0L1306](#)



Sysconfig entrance for I2C setting

Step1:



Step2:

2C (1 of 2 Added) + ADD REMOVE ALL

<input checked="" type="checkbox"/>	I2C_0	✕
Name	I2C_0	
Selected Peripheral	I2C1	
Quick Profiles		^
Basic Configuration		^
Advanced Configuration		^
Interrupt Configuration		^
DMA Configuration		^
PinMux Peripheral and Pin Configuration		^
Other Dependencies		^

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